AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

6. (Canceled)

7. (Amended) An apparatus, comprising:

a first processor for performing scalar processing, said first processor comprising a core, a program memory and a local memory;

a second processor comprising a core, a program memory and a local memory ~~The apparatus of Claim 6,~~ wherein said second processor is the main processor of said apparatus;

a synchronizing circuit for coupling said core of said first processor to said core of said second processor; and

a memory circuit for coupling said local memory of said first processor to said local memory of said second processor.

8. (Previously presented) The apparatus of Claim 7, wherein said first processor is a microprocessor.

9. (Previously presented) The apparatus of Claim 7, wherein said second processor is a digital signal processor "DSP".

10. (Currently amended) An apparatus, comprising:

a first processor for performing scalar processing, said first processor comprising a core, a program ~~The apparatus of Claim 6, wherein said program memory of said first processor is~~ ROM memory and a local memory;

a second processor comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said first processor to said core of said second processor; and

a memory circuit for coupling said local memory of said first processor to said local memory of said second processor.

11. (Currently amended) The apparatus of Claim 7~~6~~, wherein said local memory of said first processor is RAM memory.

12. (Currently amended) The apparatus of Claim 7~~6~~, wherein said program memory of said second processor is ROM memory.

13. (Currently amended) The apparatus of Claim 7~~6~~, wherein said local memory of said second processor is RAM memory.

14. (Currently amended) The apparatus of Claim 7~~6~~, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is physically separate from said first and second processors.

15. (Currently amended) The apparatus of Claim 7~~6~~, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is a DPRAM memory.

17. (Currently amended) The apparatus of Claim 7~~6~~, wherein said synchronizing circuit ensures that only one of said first and second processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time.

19. (Currently amended) The apparatus of Claim 7~~6~~, wherein an instruction set is provided to said first processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions:

integers corresponding to arithmetic and logic operations on integer numbers;

transfer corresponding to the transfer operations between a register in said protocol processor and memory; and

monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said first processor.

34. (Currently amended) The apparatus of Claim 7~~6~~, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing.

35. (Canceled)

36. (Previously presented) An apparatus, comprising:

a first processor comprising a core, a program memory and a local memory;

a second processor comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said first processor to said core of said second processor; and

one and only one common memory coupling said local memory of said first processor to said local memory of said second processor.

37. (Previously presented) An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor.

38. (Previously presented) An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory, said protocol processor being suited to execute tasks to which the main processor is not suited;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

a common memory coupling said local memory of said main processor to said local memory of said protocol processor.

39. (Previously presented) An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory, said protocol processor being suited to execute tasks to which the main processor is not suited;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor.